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REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-15 are pending in this application. No claims are amended herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. §§ 103

1. The Examiner has rejected claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Yu et al. (U.S. Patent No. 6,004,883; hereinafter "Yu") in view of Hopper et al. (U.S. Patent No. 6,030,901; hereinafter "Hopper") and Avanzino et al. (U.S. Patent No,. 5,691,238; hereinafter "Avanzino").

2. The Examiner has rejected claims 8-15 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang et al. (U.S. Patent No. 6,027,995; hereinafter "Chiang").

Applicant acknowledges the teachings of Yu, Hopper Avanzino and Chiang as cited by the Examiner.

In response applicant asserts that applicant's claim 1 and claim 8 may not properly be rejected under 35 U.S.C.§ 103(a) as being unpatentable over the foregoing combinations of references which include Yu, Hopper, Avanzino and Chiang insofar as each and every limitation

within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within Yu, Hopper, Avanzino, Chiang or any combination thereof.

In that regard, applicant asserts that there is absent within Yu, Hopper, Avanzino, Chiang or any combination thereof a disclosure of a method for forming a dual damascene aperture or a method for forming a dual damascene structure which employs a patterned first dielectric layer and a blanket second dielectric layer formed of a corresponding first dielectric material and second dielectric material each having a dielectric constant less than about 4.0, where the first dielectric material serves as an etch stop with respect to the second dielectric material.

Applicant in particular notes that while the Examiner accurately cites Hopper as disclosing a multiplicity of low dielectric constant dielectric materials for forming patterned low dielectric constant dielectric layers which may define dual damascene apertures which may be filled employing dual damascene methods, Hopper's dual damascene structure (Fig. 2) apparently illustrates with respect to a dual damascene aperture a patterned dielectric layer formed of a single dielectric material rather than a laminated pair of dielectric materials with intrinsic etch stop characteristics.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within Yu, Hopper, Avanzino, Chiang or any combination thereof, applicant asserts that claim 1 and claim 8 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over any combination of references predicated upon Yu, Hopper, Avanzino and Chiang.

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Since all remaining claims within this application are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 and claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over any combination of references predicated upon Yu, Hopper, Avanzino and Chiang.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of: (1) claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino; and (2) claims 8-15 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang, be withdrawn.

Other Considerations

Applicant acknowledges the additional prior art of record cited by the Examiner but not employed in rejecting applicant's invention, including (1) Cheek et al. (U.S. Patent No. 5,935,766); and (2) Nguyen et al. (U.S. Patent No. 6,043,164), as generally pertinent to applicant's invention.

No fee is due as a result of this Response.

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SUMMARY

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed at least in part towards a method for forming a dual damascene aperture through a dielectric layer. Applicant's method employs a patterned first dielectric layer and a blanket second dielectric layer formed of a corresponding first dielectric material and second dielectric material each having a dielectric constant of less than about 4.0, where the first dielectric material serves as an intrinsic etch stop with respect to the second dielectric material. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested. Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

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2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. The method of claim 1 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

5. The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

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8. A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

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9. The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. The method of claim 8 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

12. The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method.